Amendments to the Specification

Please replace the title as follows:

FERROELECTRIC MEMORY DEVICE~~, METHOD OF MANUFACTURING THE SAME, AND EMBEDDED DEVICE~~

Please add the following paragraph between the title and the first line of text as follows:

This is a Division of Application No. 09/934,550 filed August 23, 2001. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.

Please replace the paragraph beginning on page 2, line 25, with the following rewritten paragraph:

(1) The ferroelectric layer may be disposed linearly along the first signal electrodes. Specifically, the ferroelectric layer may be selectively disposed over the first signal electrodes. In this case, since the ferroelectric layer is formed linearly along the first signal electrodes, the parasitic capacitance or load capacitance of the second signal electrodes can be decreased.

Please replace the paragraph beginning on page 3, line 22, with the following rewritten paragraph:

(2) The ferroelectric layer may be disposed linearly along the second signal electrodes. Specifically, the ferroelectric layer may be selectively disposed under the second signal electrodes. In this case, since the ferroelectric layer is formed linearly along the second signal electrodes, the parasitic capacitance or load capacitance of the first signal electrodes can be decreased.

Please replace the paragraph beginning on page 4, lines 9-14, with the following rewritten paragraph:

(3) The ferroelectric layer may be disposed only in the intersection regions between the first signal electrodes and the second signal electrodes. In this case, since the ferroelectric layer is formed in the smallest region, the parasitic capacitance or load capacitance of the signal electrodes can be further decreased.

Please replace the paragraph beginning on page 11, lines 6-9, with the following rewritten paragraph:

The method may comprise a step (b-5) of forming insulation layers between the first signal electrodes after the step (b-1), and

upper surfaces of the insulation layers may be on the same level as upper surfaces of the first signal electrodes.

Please replace the paragraph beginning on page 20, line 25, with the following rewritten paragraph:

The ferroelectric memory device according to the second embodiment differs from the first embodiment in that the ferroelectric layer 14 is formed linearly along the second signal electrodes 16. The parasitic capacitance or load capacitance of the first signal electrodes 12 can be decreased by forming the ferroelectric layer 14 linearly. The linear ferroelectric layer 14 may be formed by patterning using a mask used to pattern the second signal electrodes 16 as described later.

Please replace the paragraph beginning on page 21, lines 6-18, with the following rewritten paragraph:

A dielectric layer 18 is formed between laminates consisting of the ferroelectric layer 14 and the second signal electrode 16 so as to cover exposed areas of the base 10 and the first

signal electrodes 12. The dielectric layer 18 preferably has a dielectric constant lower than that of the ferroelectric layer 14. The parasitic capacitance or load capacitance of the second signal electrodes 16 can be decreased by allowing the dielectric layer 18 having a dielectric constant lower than that of the ferroelectric layer 14 to be interposed between the laminates consisting of the ferroelectric layer 14 and the second signal electrode 16. As a result, a read or write operation of the ferroelectric memory device 1000 can be performed at a higher speed.

Please replace the paragraph beginning on page 27, lines 1-13, with the following rewritten paragraph:

The ferroelectric layer 14 is selectively formed on the first signal electrodes 12. Surface-modifying layer 22 is formed on the base 10 between the first signal electrodes 12. The dielectric layer 18 is formed on the surface-modifying layer 22. The dielectric layer 18 preferably has a dielectric constant lower than that of the ferroelectric layer 14. The parasitic capacitance or load capacitance of the second signal electrodes 16 can be decreased by allowing the dielectric layer 18 having a dielectric constant lower than that of the ferroelectric layer 14 to be interposed between laminates consisting of the first signal electrode 12 and the ferroelectric layer 14. As a result, read or write operations of the ferroelectric memory device can be performed at a higher speed.

Please replace the paragraph beginning on page 41, lines 7-18, with the following rewritten paragraph:

The dielectric layer 180 and the dielectric layer which is optionally formed preferably have a dielectric constant lower than that of the ferroelectric layer 14. The parasitic capacitance or load capacitance of the first signal electrodes 12 and the second signal electrodes 16 can be decreased by allowing the dielectric layer having a dielectric constant lower than that of the ferroelectric layer 14 to be interposed between the laminates consisting

of the first signal electrode 12 and the ferroelectric layer 14 and between the laminates consisting of the ferroelectric layer 14 and the second signal electrode 16. As a result, a read or write operation of the ferroelectric memory device can be performed at a higher speed.

Please replace the paragraph beginning on page 41, lines 19-25, with the following rewritten paragraph:

In the present embodiment, the ferroelectric layer 14 which makes up the ferroelectric capacitors 20 are formed only in the intersection regions between the first signal electrodes 12 and the second signal electrodes 16. According to this configuration, the parasitic capacitance or load capacitance of both the first signal electrodes 12 and the second signal electrodes 16 can be decreased.